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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,481	09/28/2001	Nathan Y. Moyal	INTL-0552-US (P11111)	6467

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NGUYEN, HAIL

[REDACTED] ART UNIT

[REDACTED] PAPER NUMBER

2816

DATE MAILED: 01/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/966,481	MOYAL, NATHAN Y.
	Examiner Hai L. Nguyen	Art Unit 2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 13 November 2002.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 11-13 and 16-43 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 11-13, 16-18 and 20-43 is/are rejected.

7) Claim(s) 19 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 28 September 2001 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Response to Amendment

1. The amendments received on 11/13/02 have been reviewed and considered with the following results:

As to the objections to the specification, Applicant's clarifications have overcome the objections, as such; the objections to the specification have been withdrawn.

As to the rejections to the claims, under 35 U.S.C. 112, 1st and 2nd paragraphs, Applicant's amendments have overcome the rejections, as such, the rejections have been withdrawn.

As to the prior art rejections to claims 1-20, Applicant's amendments have overcome the rejection, as such; the prior art rejections to claims 1-20 have been withdrawn. However, applicant's amendments necessitate a new action on the merits appears below.

As to the prior art rejections to claims 21-30, the arguments and/or comments by the applicant have been carefully reviewed, but are not persuasive. In view of the new amendment, a new action on the merits appears below.

The response to applicant's arguments is addressed as set forth below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 11, 13, 16-18, 20-22, 25-32, and 34-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Conary (US 5,570,050; previously cited).

With regard to claims 11 and 40, Conary discloses in Fig.6 an integrated circuit, and a method of use thereof, comprising an activation circuit (600) to determine whether a supply voltage (401, 601) reaches a predetermined level; a pulse generator (400) to generate pulses (402, 700) to indicate that a supply voltage is ramping up and to terminate the generation of the pulses after the supply voltage reaches a predetermined level (see column 6, lines 40-56); and a feedback path (from 402 to 622, through 300 and 500) to provide an output of the pulse generator to the activation circuit, the feedback path including an inverter (500) to create a high signal in response to a low signal on the feedback path.

With regard to claim 13, the integrated circuit includes a level detector (300) that detects when a voltage is above at least two transistor threshold voltages, the level detector operative to control the pulse generator (column 5, line 30 through column 6, line 11).

With regard to claims 16 and 41, the integrated circuit includes a pair of transistors (440 and 454) that must both conduct in order to generate the pulse (when the power supply voltage is applied and is not in the first state).

With regard to claims 17 and 42, the integrated circuit includes a capacitor circuit (416) to enable the supply voltage to reach a designated output level (see column 6, line 40 through column 7, line 2).

With regard to claims 18 and 43, the integrated circuit includes a hysteresis sense stage (610, 652, 420) coupled to the capacitor circuit (see column 6, line 40 through column 7, line 2).

4. With regard to claim 20, the integrated circuit includes a circuit (a latch, formed by four transistors, which has input/output terminals as nodes 602 and 604) to latch the pulse generator in response to the supply voltage being in a first state (see column 6, lines 56-65).

With regard to claims 21 and 31, Conary discloses in Fig.6 a power-on reset pulse generator, and a method of use thereof, comprising a first circuit (400) to develop a pulse (700) indicating that a power supply voltage (401, 601) is not in a first state; and a second circuit (600) coupled to the first circuit to latch the first circuit in response to the power supply voltage being in the first state.

With regard to claims 22 and 32, the claimed limitation is also met by the prior art (column 5, line 40 through column 6, line 26).

With regard to claims 25 and 34, the second circuit includes a level detector (300) that detects when a voltage is above at least two transistor threshold voltages, the level detector operative to control the first circuit (column 5, line 30 through column 6, line 11).

With regard to claims 26, 27, 35, and 36, the power-on reset pulse generator comprises a feedback path (from 402 to 622, though 300 and 500), including an inverter (500) coupled in the feedback path, from the output of the first circuit to the second circuit.

With regard to claims 28 and 37, the power-on reset pulse generator includes a pair of transistors (440 and 454) that must both conduct in order to generate the pulse (when the power supply voltage is applied and is not in the first state).

With regard to claims 29 and 38, the power-on reset pulse generator includes a capacitor circuit (416) to enable the supply voltage to reach a designated output level (see column 6, line 40 through column 7, line 2).

With regard to claims 30 and 39, the power-on reset pulse generator includes a hysteresis sense stage (610, 652, 420) coupled to the capacitor circuit (see column 6, line 40 through column 7, line 2).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 12, 23, 24, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Conary in view of Ansel et al. (US 5,809,312; previously cited).

With regard to claim 12, the above discussed the integrated circuit of Conary meets all of the claimed limitations except for a logic functionality (52 in instant Fig.5) to emulate logic that is difficult to trigger and to determine whether the supply voltage has reached a level sufficient to trigger the difficult to trigger logic. Ansel et al. teaches in Fig.3 a circuit having a logic functionality (310) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that logic functionality taught by Ansel et al. with the prior art (Fig.6 of Conary) in order to ensure all of the critical integrated circuits are operating correctly.

Claims 23 and 33 are similarly rejected; note the above discussion with regard to claim 12.

With regard to claim 24, the claimed limitation is also met by the prior arts.

Response to Arguments

7. Applicant's argument with respect to the prior art rejections of claim 21 in the previous Office Action concerning that "Claim 21 calls for a second circuit coupled to the first circuit to latch the first circuit in response to the power supply voltage being in a first state. While there is a latch in the cited reference, the latch does not function to latch a first circuit that develops a pulse indicating the power supply is not in its first state. In fact, it would appear that no such first circuit is connected to the latch and, therefore, cannot be latched by the latch" is not persuasive. Fig.6 of Conary clearly shows the second circuit (600) including a latch (the latch is formed by four transistors, which has input/output terminals as nodes 602 and 604) to latch the pulse generator in response to the supply voltage being in a first state, i.e., when the supply voltage is in a first state, it causes the logic low on node 602 is then transmitted by inverter 652 as a logic high on node 470 where it turns on n-channel transistor 420. Turning on n-channel transistor 420 couples node 402 to ground placing it in a logic low state (see column 6, lines 56-65). The logic low state on node 602 causes the logic high state on node 604 where it turns on n-channel transistor (the one having a gate connected to node 604) and couples node 402 to ground. In other words, the above-described function is latching function. Therefore, the rejection to claim 21 is proper and remains.

Allowable Subject Matter

8. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not disclose or suggest an integrated circuit as recited in claim 19; and specifically the limitation directed to the activation circuit (40a in instant Fig.7) includes an inverter (64a) coupled to the gate of a load transistor(66a), a second transistor (68) coupled to the load transistor and a third transistor (70a) coupled between the load transistor and the first transistor.

Conclusion

9. Applicant's amendment necessitated the new rejections presented in this Office action.

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

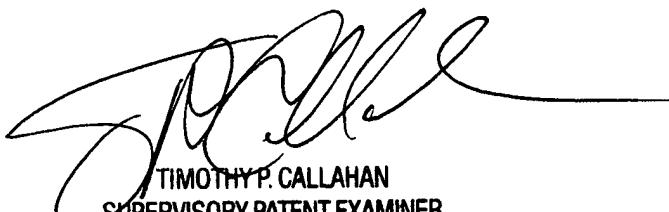
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 703-306-9178 and Right Fax number is 703-746-3951. The examiner can normally be reached on Monday-Thursday.

Art Unit: 2816

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HLN 
January 25, 2003



TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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